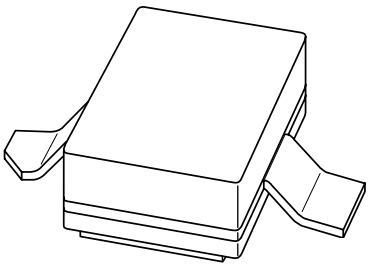
查询BLF1043供应商

DATA SHEET



BLF1043
UHF power LDMOS transistor

Objective specification
Supersedes data of 2000 Feb 17

2000 Feb 23

Philips
Semiconductors

PHILIPS

UHF power LDMOS transistor BLF1043

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source

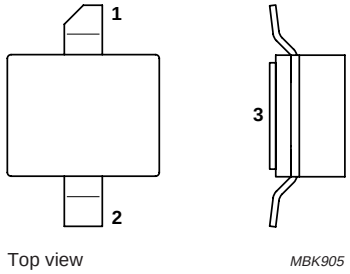


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	10 (PEP)	>16	>35	≤–30
CW, class-AB (1-tone)	960	26	10	>16	>45	–

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	75	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	2.2	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	tbf	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; note 1	4.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.4	K/W

Note

1. Thermal resistance is determined under RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.2 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 20 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	0.15	µA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	3	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	1	µA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 0.75 A	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.75 A	–	1.2	–	Ω
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	11	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	9	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	0.6	–	pF

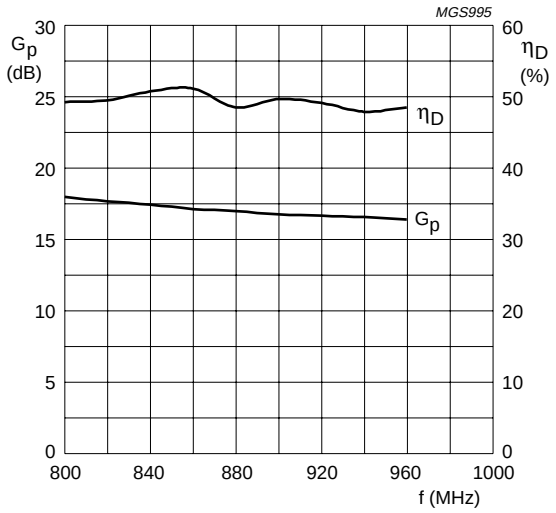
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	25	10 (PEP)	>16	>35	≤–30
CW, class-AB (1-tone)	960	26	25	10	>16	>45	–

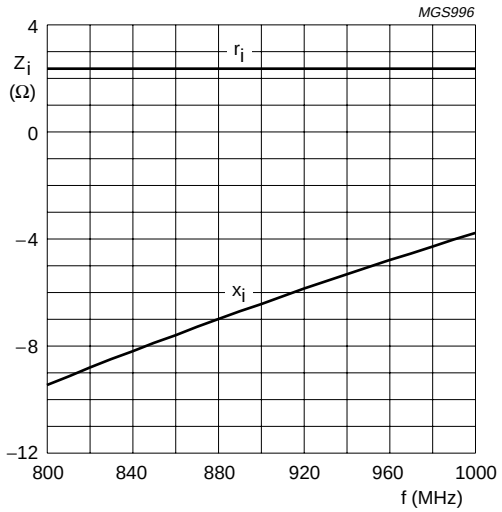
Ruggedness in class-AB operation

The BLF1043 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.



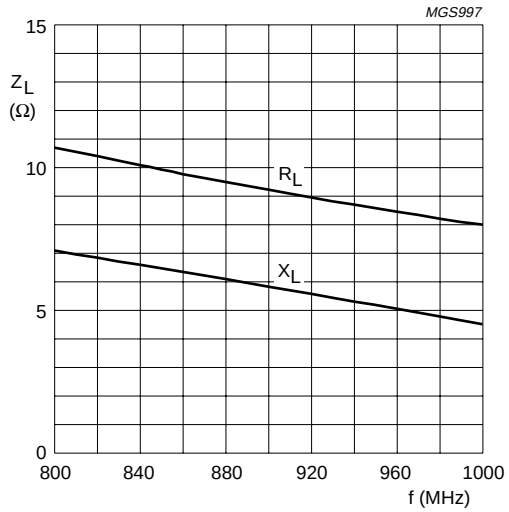
Class-AB operation; V_{DS} = 26 V; I_{DQ} = 80mA; P_L = 10 W (PEP).

Fig.2 Power gain and efficiency as functions of frequency, typical values.



V_{DS} = 26 V; I_{DQ} = 80 mA; P_L = 10 W (PEP); $T_h \leq 25$ °C.
Impedance measured at reference planes (see Fig.5).

Fig.3 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 80 mA; P_L = 10 W (PEP); $T_h \leq 25$ °C.
Impedance measured at reference planes (see Fig.5).

Fig.4 Load impedance as a function of frequency (series components); typical values.

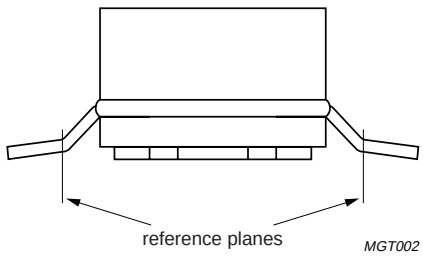


Fig.5 Measuring reference planes SOT538A.

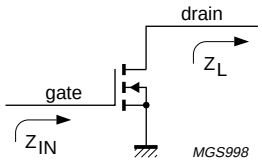


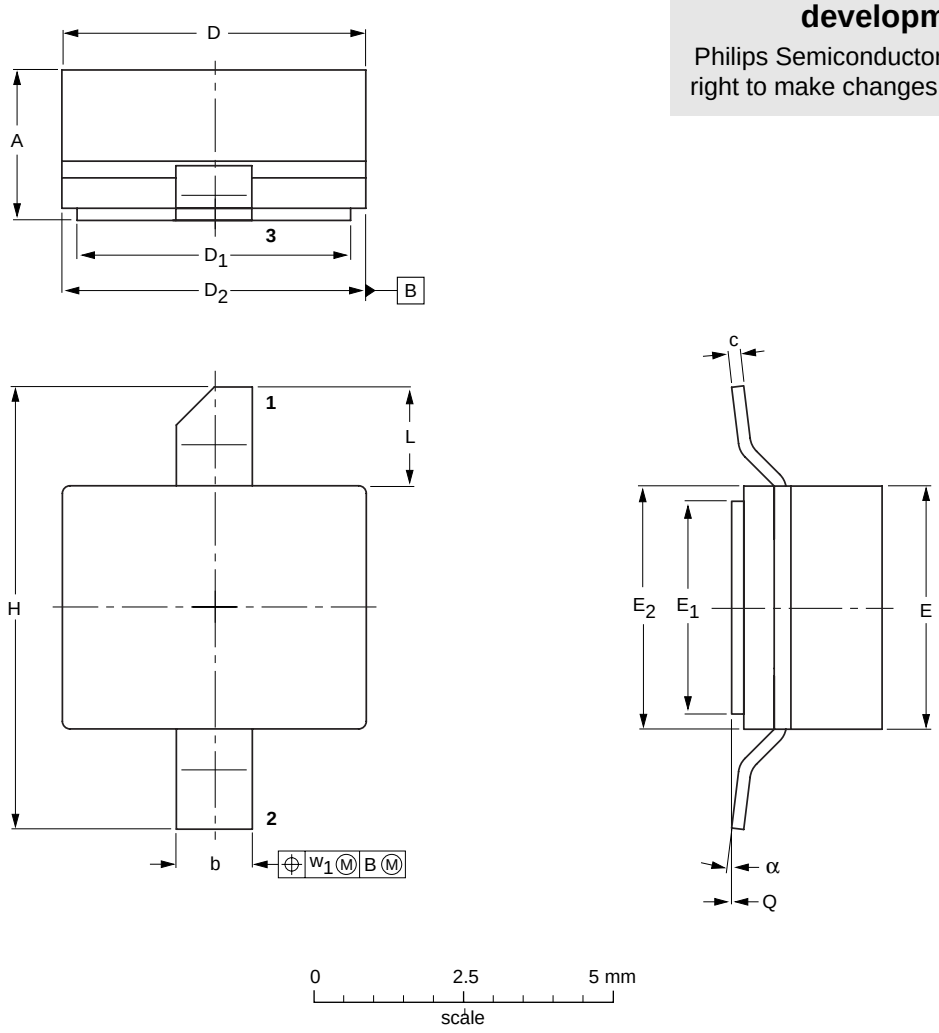
Fig.6 Definition of transistor impedance.

PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads **SOT538A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	Q	w_1	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.41 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.213 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT538A						99-03-30

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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